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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,505	09/19/2003	Federico Caccavale	UK02-013	9182

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CORNING INCORPORATED
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EXAMINER	
SONG, SARAH U	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,505	CACCAVALE ET AL.	
	Examiner	Art Unit	
	Sarah Song	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 September 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0903.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The prior art documents submitted by the applicant in the Information Disclosure Statement filed on September 19, 2003 have all been considered and made of record (note the attached copy of form PTO-1449).

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference sign "23" on page 7, line 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1, 3, 5, 6, 8-10 rejected under 35 U.S.C. 103(a) as being unpatentable over Kulishov (U.S. Patent 6,353,690 cited by Applicant) in view of Fournier et al. (U.S. Patent 4,750,800 cited by Applicant).**

6. Regarding claims 1, 3, 5, 6 and 8-10, Kulishov discloses an integrated optical chip having a crystalline structure cut along parallel principal crystallographic planes and a thickness less than 0.25mm (column 5, lines 50-54), an optical signal pathway 22 being disposed generally longitudinally in one of the cut surfaces of the chip, wherein the chip is attached to a substrate material 26, characterized by a grounding plane disposed between the chip and substrate providing an electrically conductive path (metallized layer) between opposite lateral surfaces of the chip (Figure 9c; column 8, lines 36-39).

7. Kulishov does not expressly disclose the substrate of a material having similar coefficients of thermal expansion in said principal crystallographic plane or having a thickness up to 1.0mm. Kulishov also does not disclose attachment of the chip to the substrate with an adhesive.

8. Fournier et al. discloses an integrated optical chip comprising a lithium niobate chip mounted on a lithium niobate substrate 14, wherein the thickness of the substrate is about 10 times the thickness of the chip. Fournier et al. also discloses attachment of the chip to the substrate with an adhesive 48.

9. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the substrate thickness of Kulishov of about 10 times the

thickness of the chip (i.e. up to 1.0mm), the substrate comprising the same material and therefore exhibiting similar coefficient of thermal expansion, for the purpose of reducing thermally induced stress (column 4, lines 6-10 of Fournier et al.). It would also have been obvious to one having ordinary skill in the art at the time the invention was made to attach the chip of Kulishov to the substrate of Kulishov with an adhesive for the purpose of reducing stress transmission (column 3, lines 45-50 of Fournier et al.).

10. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kulishov in view of Fournier et al. as applied to claim 1 above, and further in view of Shafer et al. (U.S. Patent 6,044,184 cited by Applicant).**

11. Regarding claim 2, the claimed invention is disclosed as discussed above, except wherein the lateral surfaces of the chip have an electrically conductive coating.

12. Shafer et al. discloses an integrated optical chip wherein the lateral surfaces of the chip have an electrically conductive coating (Abstract).

13. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the lateral surfaces of the chip of Kulishov in view of Fournier et al. for the purpose of preventing a charge differential between the surfaces.

14. **Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kulishov in view of Fournier et al. as applied to claim 3 or 6 as applicable above, and further in view of Shaw et al. (*Low Cost PackagingTtechniques for Active Waveguide Devices.*)**

15. Regarding claims 4 and 7, the claimed invention is disclosed as discussed above, except wherein the substrate material comprises a ceramic/thermoset polymer composite, and wherein the adhesive comprises epoxy resin.

16. Shaw et al. discloses an integrated optical chip wherein the substrate material comprises a ceramic/thermoset polymer composite, and wherein the adhesive comprises epoxy resin (page 743).

17. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the ceramic/thermoset polymer composite and also to provide adhesive comprising epoxy resin for the purpose of providing improved structural characteristics to the device, and to eliminate problems due to poor adhesion.

18. **Claims 11-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kulishov in view of Fournier et al., Shaw et al. and Shafer et al.**

19. Regarding claims 11, Kulishov discloses of manufacturing an integrated optical chip, the chip having a crystalline structure cut along parallel principal crystallographic planes and a thickness of less than 1.0 mm, an optical signal pathway being disposed in one of the cut surfaces of the chip, the method comprising the steps of: (i) forming at least one optical signal pathway 22 in a first surface of a crystalline wafer cut along parallel principal crystallographic planes to a thickness less than 1 mm (column 5, lines 50-54); (ii) applying an electrically conductive layer to a second surface of the crystalline wafer opposite to that of the optical signal pathway (see Figure 9c); (iii) attaching a substrate material slab 26 to the said conductive layer on said crystalline wafer.

20. Kulishov does not expressly disclose the substrate of a material having similar coefficients of thermal expansion in said principal crystallographic plane or having a thickness up to 1.0mm. Kulishov also does not disclose attachment of the chip to the substrate with an adhesive.

21. Fournier et al. discloses an integrated optical chip comprising a lithium niobate chip mounted on a lithium niobate substrate 14, wherein the thickness of the substrate is about 10 times the thickness of the chip. Fournier et al. also discloses attachment of the chip to the substrate with an adhesive 48.

22. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the substrate of Kulishov of the same material as the chip, having a similar coefficient of thermal expansion and having a thickness of about 10 times the thickness of the chip (i.e. up to 1.0mm) for the purpose of reducing thermally induced stress (column 4, lines 6-10 of Fournier et al.). It would also have been obvious to one having ordinary skill in the art at the time the invention was made to attach the chip of Kulishov to the substrate of Kulishov with an adhesive for the purpose of reducing stress transmission (column 3, lines 45-50 of Fournier et al.).

23. Kulishov also does not expressly disclose the method comprising dicing a composite chip on substrate from the wafer-slab structure, the said composite chip comprising a substrate and at least one optical signal pathway extending generally longitudinally with respect to the composite chip.

24. Shaw et al. discloses a method of manufacturing an integrated optical device comprising the step of dicing a composite chip on substrate from the wafer-slab structure, the said composite

chip comprising a substrate and at least one optical signal pathway extending generally longitudinally with respect to the composite chip (page 744, column 2, through 745, column 1).

25. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to manufacture the device as discussed above with regard to Kulishov and Fournier et al., and further comprising the step of dicing a composite chip on substrate from the wafer-slab structure, the said composite chip comprising a substrate and at least one optical signal pathway extending generally longitudinally with respect to the composite chip as taught by Shaw et al.

26. One of ordinary skill in the art would have been motivated to make the modification for the purpose of providing a low cost process for mass production (top of page 756, Shaw et al.)

27. Lastly, Kulishov does not expressly disclose the step of applying an electrically conductive path to lateral surfaces of the said composite chip.

28. Shafer et al. discloses the step of applying an electrically conductive coating to lateral surfaces of the chip (Abstract).

29. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the step of applying an electrically conductive coating to lateral surfaces of the chip as discussed above for the purpose of preventing a charge differential between the surfaces.

30. Regarding claim 12, the claimed method is disclosed except wherein the surface of the composite chip on which the optical signal pathway is formed and the longitudinal end surfaces between which the optical signal pathway extends are masked prior to applying an electrically conductive path. However, it is well known in the art to provide masking before a coating

process for preventing misapplication of the coating on undesired areas. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to mask the surface of the composite chip on which the optical signal pathway is formed and the longitudinal end surfaces between which the optical signal pathway extends to preserve the optical characteristics of the optical pathway.

31. Regarding claim 13,the crystalline wafer comprises lithium niobate.

32. Regarding claim 14, 16, 17 and 19 Shaw et al. discloses a substrate material comprising a ceramic/thermoset polymer composite, and bonding with an electrically conductive adhesive comprising epoxy resin. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the ceramic/thermoset polymer composite and also to provide adhesive comprising an electrically conductive epoxy resin for the purpose of providing improved structural characteristics to the device, and to eliminate problems due to poor adhesion. It is noted that the electrically conductive layer is a metallized grounding plane (Figure 9c; column 8, lines 36-39).

33. Regarding claim 15, the substrate material comprises the same material as that of the chip, as taught by Fournier et al., would have been obvious for reducing thermally induced stresses.

34. Regarding claim 18, Shafer et al. discloses the metallization to be deposited by vacuum deposition or sputtering, but does not expressly disclose an electron beam evaporation process. An electron beam evaporation process would have been obvious since applicant has not disclosed that the particular type of deposition solves any problem or is for a particular purpose and it appears that the invention would perform equally well with any deposition method.

35. Regarding claim 20, the electrically conductive path provided by Shafer et al. is a metallized layer.

36. Regarding claim 21, composite metal layers are well known in the art for improving adhesion of the metal layers and therefore would have been obvious to one of ordinary skill in the art at the time the invention was made.

37. Regarding claim 22, Shafer et al. discloses the metallization to be deposited by vacuum deposition or sputtering, but does not expressly disclose an electron beam evaporation process. An electron beam evaporation process would have been obvious since applicant has not disclosed that the particular type of deposition solves any problem or is for a particular purpose and it appears that the invention would perform equally well with any deposition method.

Conclusion

38. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarah Song whose telephone number is 571-272-2359. The examiner can normally be reached on M-Th 7:30am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on 571-272-2344. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sarah Song
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